TARGETED FAULT TOLERANCE BY SPECIAL CPU INSTRUCTIONS

ABSTRACT OF THE DISCLOSURE

One embodiment disclosed relates to a microprocessor for targeted fault-tolerant computing. The microprocessor's decode circuitry is configured to decode a fault-tolerant version of an instruction and a non-fault-tolerant version of the instruction distinctly from each other. The microprocessor's execution circuitry is configured to execute the fault-tolerant version of the instruction with redundancy checking and to execute the non-fault-tolerant version of the instruction without redundancy checking.